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Third Workshop on Dependable and Secure Nanocomputing

Monday June 29, 2009, Estoril, Lisbon, Portugal **www.laas.fr/WDSN09**

Organizers: **Jean Arlat, LAAS-CNRS, Université de Toulouse, France**
Cristian Constantinescu, AMD, Fort Collins, CO, USA
Ravishankar K. Iyer, UIUC, Urbana-Champaign, USA
Johan Karlsson, Chalmers University of Technology, Göteborg, Sweden
Michael Nicolaïdis, TIMA, Université de Grenoble, France

— Final Program —

Time / Session	Program
8:30 - 10:00 **Session 1** ***Opening and Invited Talks***	***Moderator: Jean Arlat*** • Introduction to the Workshop ***Jean Arlat**, Cristian Constantinescu, Ravishankar K. Iyer, Johan Karlsson, Michael Nicolaïdis* • Dependable Design in Nanoscale CMOS Technologies: Challenges and Solutions *Vikas Chandra, ARM R&D, San Jose, CA, USA* • Trading Off Dependability and Cost for Nanoscale High Performance Microprocessors: The Clock Distribution Problem *Cecilia Metra, Università di Bologna, Italy*
10:00 - 10:30	***Coffee Break***
10:30 - 12:00 **Session 2** ***Reliability Issues and Assessment***	***Moderator: Johan Karlsson*** • Scaling Effects on Neutron-Induced Soft Error in SRAMs Down to 22nm Process ***Eishi Ibe**, Hitoshi Taniguchi, Yasuo Yahagi, Ken-ichi Shimbo, Tadanobu Toba; Hitachi Ltd, Yokohama, Japan* • On CMOS Circuit Reliability from MOSFETs and Input Vectors ***Valeriu Beiu**[1,2], Walid Ibrahim[1,3]; [1] UAE University, Al-Ain, UAE; [2] University of Ulster, Londonderry, UK; [3] Carleton University, Ottawa, Canada* • Impact of Manufacturing Defects on Carbon Nanotube Logic Circuits *Daniel Gil, **David de Andrés**, Juan-Carlos Ruiz, Pedro Gil; Universidad Politécnica de Valencia, Spain* • Enhanced Fault Coverage Analysis Using ABVFI ***Scott Bingham**, John Lach; University of Virginia, Charlottesville, USA*
12:00 - 13:30	***Lunch***
13:30 - 15:00 **Session 3** ***Resilience Enhancement Techniques***	***Moderator: Michael Nicolaïdis*** • Achieving Degradation Tolerance in a Hardware Accelerator with Parallel Functional Units ***Tomohiro Yoneda**, National Institute of Informatics, Tokyo; Masashi Imai, University of Tokyo; Hiroshi Saito, University of Aizu; Atsushi Matsumoto, Tohoku University, Sendai; Japan* • Software Mechanisms for Tolerating Soft Errors in an Automotive Brake-controller ***Daniel Skarin**, Johan Karlsson; Chalmers University of Technology, Göteborg, Sweden* • Power Efficient Redundant Execution for Chip Multiprocessors ***Pramod Subramanyan**[1], Virendra Singh[1], Kewal Saluja[2], Erik Larsson[3]; [1] Indian Institute of Science, Bangalore, India; [2] University of Wisconsin-Madison, USA; [3] Linköping University, Sweden* • On the Stability and Robustness of Non-Synchronous Circuits with Timing Loops *Matthias Függer, Gottfried Fuchs, Ulrich Schmid, **Andreas Steininger**; Vienna University of Technology, Austria*
15:00 - 15:30	***Coffee Break***
15:30 - 17:00 **Session 4** ***Panel: Scaling Towards Nanometer Size Devices: Issues and Solutions*** ***and Closing***	***Moderator: Cristian Constantinescu*** ***Panelists:*** • *Jacob A. Abraham, University of Texas, Austin, USA* Dependable Systems with Nanometer Scale Technologies: What is Different? • *Valeriu Beiu UAE, University, Al-Ain, UAE and University of Ulster, Londonderry, UK* Why Brain-inspired Architectures Could Save the Day? • *Helia Naeimi, Intel Corporation, Santa Clara, CA, USA* Cross-Layer Resiliency for Nano-scale Technology • *Arun Somani, Iowa State University, Ames, USA* Aggressive and Adaptive Mitigation Techniques may be Key to the Solution • *Seongmoon Wang, NEC Laboratories America, Princeton, NJ, USA* Now Silicon is Cheap, but Testing is Expensive ***Workshop Wrap-Up***

NB. Contributions with several authors: ***Presenter*** shown in Boldface characters

Update: Tuesday July 31, 2009